Advanced Research in Electrical and Electronic Engineering
Print ISSN: 2349-5804; Online ISSN: 2349-5812 Volume 2, Number 7 April-June (2015) pp. 9-11

http://www.krishisanskriti.org/areee.html

Soft Switching PWM Three-Level DC-DC Converter

Kavya Shree N[1] and Arpitha Raju B[2]

[1]Department of Electrical and Electronics Dr. Ambedkar Institute of Technology Bengaluru
[2]Dr. Ambedkar Institute of Technology Bengaluru
E-mail: [1]himagirishail@yahoo.com, [2]rajuarpitha@gmail.com

Abstract*—*This paper proposes soft switching solution to a pulse width modulation (PWM) three-level (TL) dc-dc converter. The proposed converter topologies have the following advantages: all power switches have to withstand only half of the input voltage, primary clamping devices such as clamping diodes, flying capacitors are not required to clamp the off state voltage. The converter can achieve ZVS for the leading switches and ZCS or ZVS for the lagging switches. ZVZCS converter which combines the advantage of both zero voltage and zero current switching converter is selected. ZCS is a better solution for converters with IGBTs because of large tailing current during switching commutation as dc-dc converters are usually operated at high input voltage. The simulation study is carried out in MATLAB/ SIMULINK to predict the performance of the proposed scheme.

1. INTRODUCTION

The idea of having circuits that generate three-level (TL) voltage waveforms can be traced back to two US patents granted in the early 1960s. It should be emphasized that the application of the TL technique does not create a TL voltage state in the case of dc-dc converters. The technique has been applied to dc-dc converter by Pinheiro and Barbi to reduce the voltage stress of the switches.

A novel PWM TL dc-dc converter was first proposed in 1992 [1] to lower the voltage stress applied on the switches. The authors in [3] proposed a new four switch full bridge dc-dc converter well suited for power converters operating at high input voltage which features $V_{in}/2$ on each switch, capacitive turn-off and zero-voltage turned on. The topology reduces turn-off switching losses by providing capacitive snubbing. Paper [2] presents classification of soft-switching PWM TL converter according to the soft-switching type of the leading and the lagging switches: 1) ZVS PWM TL converter, whose zero state operates in constant current mode. 2) ZVZCS PWM TL converter, whose zero state operates in current reset mode, the leading switches realize ZVS and the lagging switches realize ZCS.

Paper [6] presents zero-voltage and zero-current switching (ZVZCS) PWM TL dc-dc converter with freewheeling diodes and flying capacitor suitable for wide input voltage range applications. Many other good research works have been published regarding the three-level (TL) dc-dc converters which are suitable for high voltage applications [7, 8].

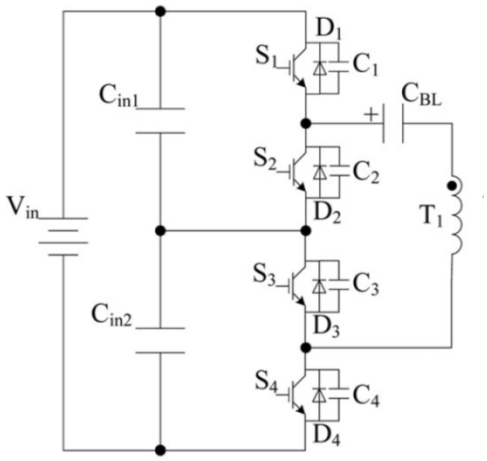


Fig. 1: PWM TL dc Converter

A PWM TL dc-dc converter is shown in the Fig.1which features $V_{in}/2$. The voltage stress of the four switches is safely sustained during the operation as the off state voltage of the switches is directly clamped by the bulky input capacitors. Compared to other clamping devices, the bulky input capacitors can absorb more resonant energy stored in the parasitic inductances, which means the active switches can be kept in the safe operating area (SOA) even under fast dynamic transition instant. The converter has simple and compact structure. Commonly, the input voltage of dc-dc converter may be 800V or higher and since the off state voltage of the switches is only half of the input voltage, lower voltage rating switches say 500-600 V can be used which improves the total power density and achieve better overall system performance.

This paper provides soft switching solution to the converter in Fig.1and presents four kinds of novel topologies. The proposed topologies have the following common features: all switches in the circuit sustain only half of the input voltage; off state voltage of the switches is directly clamped by the input capacitors and no added clamping devices such as clamping diodes and flying capacitors are required. The leading switches in each converter can only realize ZVS, while the lagging switches can achieve ZVS or ZCS in different converter.

2. SOFT SWITCHING TOPOLOGIES

The Soft switching topologies are:

1. ZVS TL PWM Converter with one CAC per module

2. ZVS TL PWM Converter with two CACs per module

3. ZVZCS TL PWM Converter

4. ZVZCS TL PWM Converter with one CAC per module

Depending on the number of switches in the converter, the switches can be divided into switching pairs. According to the different switching patterns, the switches in each switching pair can be treated as either leading switches or lagging switches. The output voltage is regulated by shifting the phase angle between the switching pairs. The energy stored in the transformer leakage inductance is utilized by the converter to achieve ZVS which is a disadvantage. There are two methods to solve this problem: 1. improved ZVS (IZVS)

2. ZCS

3. SELECTION OF TOPOLOGY

ZVS PWM combined TL dc-dc converter experience ZVS difficulty because only the energy stored in the leakage inductance of the transformer is used to achieve ZVS. In order to achieve a complete ZVS of switches down to light load, we can increase the leakage inductance of the transformer or add an external resonant inductance in series with the primary sides of the transformer. However, increased leakage inductance will cause a duty cycle loss at the secondary rectified voltage and will result in severe parasitic oscillation on the secondary side of the transformer, which will reduce the overall efficiency indirectly. PWM dc-dc converters are usually operated at high input voltage which makes IGBT more favorable than MOSFET for these converters, and ZCS technology is more suitable for converters with IGBTs because of large tailing current during switching commutation. Due to the aforementioned reasons, ZVZCS TL PWM Converter (Fig.2) is more suitable topology to achieve soft switching. Also, the circuit is simple, compact and easy to analyze in comparison with the other topologies.

Fig.2 depicts ZVZCS TL PWM Converter which consists of four switches $S_1 - S_4$, dc blocking capacitor C_{BL} which is large enough to sustain the average voltage of $V_{in}/2$. L_{lk} is the leakage inductance of T_1. D_3 and D_4 are cut-off diodes. C_{in1} and C_{in2} are dc link capacitors with same value and large enough to share the input voltage evenly i.e. $V_{cin1} = V_{cin2} = V_{in}/2$. D_{01} and D_{02} are rectifier diodes. Output filter is composed of L_0 and C_0. R_0 is the load resistance. Full wave rectifier is adopted in this topology.

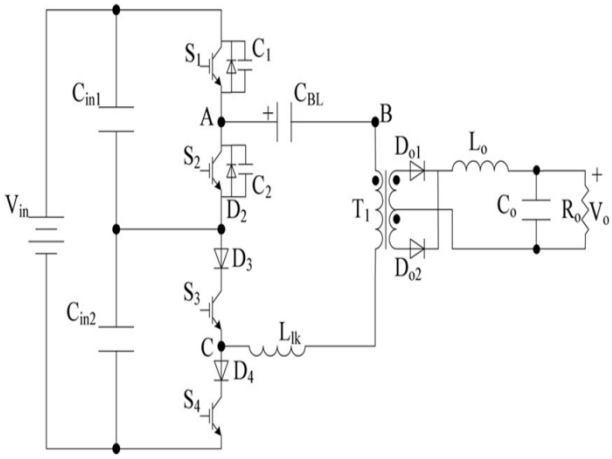


Fig. 2: ZVZCS TL PWM Converter

4. PROPOSED TOPOLOGY

4.1 Principle of operation of ZVZCS TL PWM Converter

To simplify the analysis of the circuit operation , the following assumptions are made:

1. All components are ideal.

2. Voltage ripple on the dc link capacitors can be neglected.

3. Output capacitance of each switch is of same value and represented by C_{os} in the equations.

4. Output filter and load can be considered as a constant current source.

Stage.1 [Fig. 6(a)]: Before t_0, the circuit operates in the steady condition and power is transferred from input source to the load. S_1 and S_4 are turned ON; D_{o1} is conducted while D_{o2} is OFF; the voltage of C_{BL} increases linearly with time, and the slope of V_{CBL} is given by

$$\frac{dv_{CBL}}{dt} = \frac{I_o}{k_T C_{BL}} \quad (1)$$

During this stage, $V_{BC} = V_{in} - V_{CBL}$; $V_{rect} = (V_{in} - V_{CBL})/k_T$; and $i_p = Io/k_T$

Stage 2 [Fig. 6(b)] : At instant t_0, S_1 is turned OFF at zero voltage due to the existence of C_1;V_{CBL} keeps increasing during this stage, and reaches its peak value V_{CBLP} at the end

of this stage; i_p keeps constant value of Io/k_T during this intervals, and charges C_1 and discharges C_2 linearly with time. This stage continues until V_{C1} equals to Vin/2 and V_{C2} decays to zero. The voltage of point A is given by

$$V_A(t) = V_{in} - \frac{I_0(t-t_0)}{2k_T C_{OS}}. \quad (2)$$

At instant t_1, V_A deceases to $V_{in}/2$ and the time of this interval is

$$T_{10} = \frac{k_T C_{0s} V_{in}}{I_0} \quad (3)$$

Stage 3 [Fig. 6(c)]: At instant t_1, D_2 is conducted naturally; the circuit is operated in the free-wheeling mode; both of the rectifier diodes are conducted; during this stage, S_2 must be gated on to achieve ZVS, S_2 is turned on at instant t_2; V_{rect} = 0. The voltage of C_{BL} can be treated as a constant voltage source represented as V_{CBLP} during this stage and it is fully applied to L_{lk} to reset the primary side current. The expression of i_p in this stage can be given by

$$i_p(t) = \frac{I_0}{k_T} - \frac{V_{CBLP} - \frac{V_{in}}{2}}{L_{lk}}(t-t_1) \quad (4)$$

This stage ends until i_p decays to zero, and the time of this stage is

$$T_{31} = \frac{I_0 L_{lk}}{k_T (V_{CBLP} - \frac{V_{in}}{2})} \quad (5)$$

Stage 4 [Fig. 6(d)]: At instant t_3, i_p decays to zero. Due to the existence of D_4, the primary current cannot be conducted in the reverse direction. After the instant of t_3, i_p keeps the value zero, so S_4 can achieve ZCS turned off. The voltage of C_{BL} keeps constant.

Stage 5 [Fig. 6(e)]: At instant t_4, S_3 is gated ON, and S3 can achieve ZCS turned on due to the existence of the L_{lk}; S_2 has been turned on at instant t_2; i_p increases linearly with time in the reverse direction, and the circuits is still in the free-wheeling modes until i_p reaches to $-I_o/k_T$. i_p in this stage is given by

$$i_p(t) = -\frac{v_{CBL}}{L_{lk}}(t - t_4) \quad (6)$$

The voltage of C_{BL} decreases due to discharging current i_p

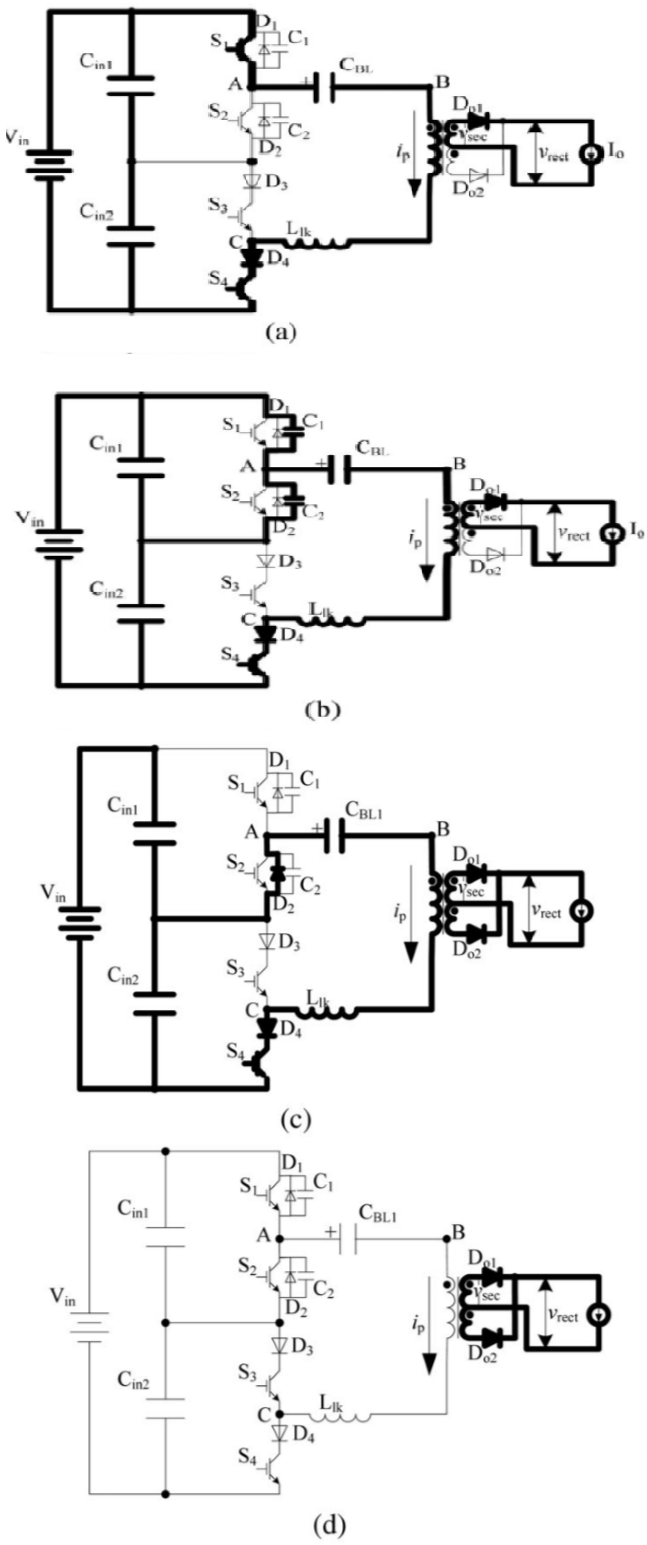
$$V_{CBL}(t) = V_{CBLP} - \int_{t_4}^{t} i_p(t)dt \quad (7)$$

This interval ends until $i_p = -I_o/k_T$, so the time of this interval can be computed according to the above equation.

Stage 6 [Fig. 6(f)]:

At instant t_5, i_p reaches to $-I_o/k_T$; the free-wheeling mode is over. Primary powers the load from the energy stored in C_{BL}

through S_2, D_3, S_3, the transformer, and output rectifier and filter. $V_{BC} = -V_{CBL}$; $V_{rect} = V_{CBL}/k_T$; $i_p = -I_o/k_T$.



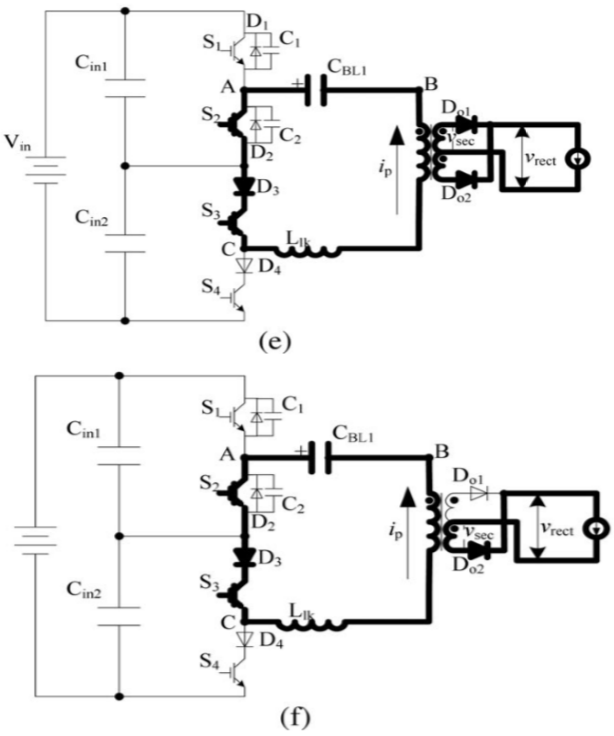


Fig. 3: Equivalent circuits of ZVZCS TL PWM Converter

4.2 Description of the Blocking Capacitor

In order to make i_p decay to zero in the zero state, a blocking voltage source could be inserted in series with the primary winding of the transformer. The blocking voltage source is nothing but the blocking capacitor $C_{BL.}$ When the upper pair of switches conducts, i_p charges C_{BL} and discharges C_{BL} when the lower pair of switches conduct. During zero state, as i_p decays and it is not enough to provide load current, rectifier diodes conduct simultaneously which makes both primary and secondary voltage to be zero. The primary current flows through C_{BL} with constant value during the power transfer state and keeps zero during freewheeling intervals.

5. SIMULATION STUDY

The topology considered for simulation i.e., ZVZCS TL PWM Converter is shown in Fig 2. Simulation study is carried out using MATLAB/SIMULINK. The parameters of the topology are given in Table 1.

Table 1: Simulation parameters

Input Voltage	600 V
Output Voltage	80 V
Switching frequency	20kHz
DC link Capacitor	400mF
Blocking Capacitor	60mF
Leakage Inductance	0.1µH
L0	20µH
Co	20µF

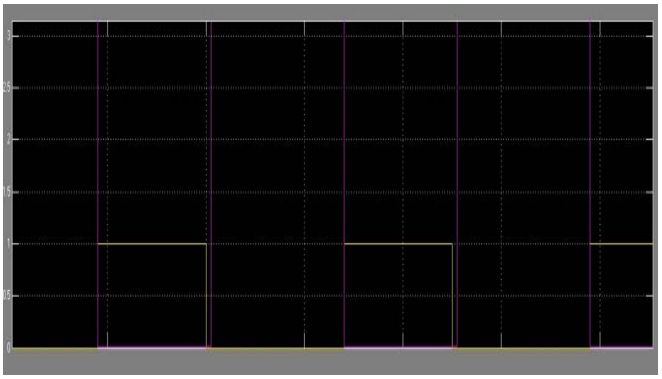


Fig. 4: Zero-voltage switching of S_1

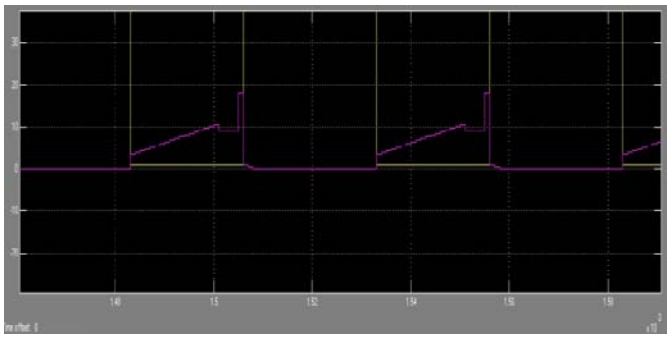


Fig. 5: Zero-current switching of S4

6. CONCLUSION

This paper provides soft switching solution to a PWM TL dc-dc converter which is simple, compact and easy to analyze. All the switches suffer a voltage stress of $V_{in}/2$ without added clamping device. The performance of the topology is validated by simulation.

REFERENCES

[1] J. R .Pinheiro and I. Barbi, “The three-level ZVS PWM converter—a new concept in high-voltage DC-to-DC conversion,” in Proc. IEEE Int. Conf. Ind. Electron. Control Instrum. Autom., 1992, pp. 173–178.

[2] X. Ruan, L. Zhou, and Y. Yan, “Soft-switching PWM three-level converters,” IEEE Trans. Power Electron., vol. 16, no. 5, pp. 612–622, Sep. 2001.

[3] I. Barbi, R. Gules, R. Redl, and N. O. Sokal, “DC/DC converter: Four switches Vpk = Vin/2, capacitive turn-off snubbing, ZV turn-on,” IEEE Trans. Power Electron., vol. 19, no. 4, pp. 918–927, Jul. 2004.

[4] X. Ruan, B. Li, Q. Chen, S. Tan, and C. K. Tse, “Fundamental considerations of three-level DC–DC converters : topologies, analyses, and control,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 55, no. 11, pp. 3733–3743, Dec. 2008.

[5] D. V. Ghodke, K. Chatterjee, and B. G. Fernandes, “ Three-phase three-level, soft switched phase shifted PWM DC-DC converter for high-power applications,” IEEE Trans. Power. Electron., vol. 23, no.3, May. 2008.

[6] F. Liu, J. Yan, and X. Ruan, “Zero-voltage and zero-current-switching PWM combined three-level DC/DC converter,” IEEE Trans. Ind. Electron., vol. 57, no. 5, pp. 1644–1654, May 2010.

[7] C. Yoon, J. Kim, and S. Choi, “Multiphase DC–DC converters using a boost-half-bridge cell for high-voltage and high-power applications,” IEEE Trans. Power Electron., vol. 26, no. 2, pp. 381–388, Feb. 2011.

[8] H. Wang, H. S.-H. Chung, and A. Ioinovici, “A new concept of high voltage DC–DC conversion using asymmetric voltage distribution on the switch pairs and hybrid ZVS–ZCS scheme,” IEEE Trans. Power Electron., vol. 27, no. 5, pp. 2242–2259, May 2012.

[9] E.Deschamps and I.Barbi, “A comparison among three-level ZVS-PWM isolated DC-to-DC converters,” in Proc. Annu. Conf. IEEE Ind. Electron. Soc., 1998, pp. 1024–1029.

[10] L. M. Tolbert and F. Z. Peng, “Multilevel converters as a utility interface for renewable energy systems,” in Proc. Power Eng. Soc. Summer Meet., 2000, vol. 2, pp. 1271–1274.